IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF NEW JERSEY

MOSAID TECHNOLOGIES INCORPORATED, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.,and SAMSUNG AUSTIN SEMICONDUCTOR, L.P. Defendants.	Civil Action No. 01-4340 (WJM)

DEFENDANTS' SECOND SUPPLEMENTAL RESPONSES TO MOSAID TECHNOLOGIES INCORPORATED'S FIRST SET OF INTERROGATORIES (2-4)

Pursuant to Rules 26(e) and 33 of the Federal Rules of Civil Procedure, Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, L.P. (collectively "Samsung"), by and through its undersigned counsel, hereby provide supplemental responses to *Mosaid Technologies Incorporated's First Set of Interrogatories* (2-4).

INTERROGATORY NO. 1:

Separately identify each SAMSUNG DRAM and SAMSUNG DRAM product, including an identification of the model or part number used by SAMSUNG.

RESPONSE TO INTERROGATORY NO. 1:

Subject to and without waiving its previously asserted general and specific objections, Samsung states that to the extent it is in possession of non-privileged documents responsive to this interrogatory, Samsung has produced such documents pursuant to Fed. R. Civ. P. 33(d). To

the extent any supplement answer to this interrogatory is needed, the information may be derived or ascertained from the documents already produced by Samsung, for example, see S 033523-036941, S 037389-041459 and other similar documents.

INTERROGATORY NO. 2:

State the dates on which each SAMSUNG DRAM and SAMSUNG DRAM product was first made, offered for sale, and sold, both in the United States and abroad; and if any devices no longer are sold in the United States, the dates on which they were last sold in the United States.

RESPONSE TO INTERROGATORY NO. 2:

Subject to and without waiving its previously asserted general and specific objections, Samsung states that to the extent it is in possession of non-privileged documents responsive to this interrogatory, Samsung has produced such documents pursuant to Fed. R. Civ. P. 33(d). The answer to this interrogatory may be derived or ascertained from the documents already produced by Samsung, for example, see S 003912-019066, S 056501-056560 and other similar documents. Samsung further states that since Samsung does not, in its ordinary course of business, keep business records according to the specified categories listed in this interrogatory, the burden of deriving or ascertaining the answer is substantially the same for Samsung as for Mosaid.

INTERROGATORY NO. 3:

State in detail each of SAMSUNG's contentions that any claims of the MOSAID patents-in-suit are invalid, unenforceable or void for any reason, providing an identification of the documents that SAMSUNG contends supports such contentions, of the factual basis for such contentions, and of each person having knowledge of that factual basis.

RESPONSE TO INTERROGATORY NO. 3:

Subject to and without waiving its previously asserted general and specific objections, Samsung responds as follows:

The Mosaid patents-in-suit are invalid for failure to satisfy the conditions of patentability set forth by the Patent Laws of the United States, Title 35, United States Code, and the Rules and Regulations of the United States Patent and Trademark Office ("USPTO"), and specifically at least Title 35 U.S.C. §§ 102, 103, 112 and/or 132. Samsung further states that the following list may include one or more references upon which Samsung relies in support of its contentions:

1. USP 3,761,899
2. USP 3,801,831
3. USP 3,942,047
4. USP 3,980,899
5. USP 4,000,412
6. USP 4,001,606
7. USP 4,037,114
8. USP 4,039,862
9. USP 4,080,539
10. USP 4,189,782
11. USP 4,208,595
12. USP 4,216,390
13. USP 4,271,461
14. USP 4,279,010
15. USP 4,307,333
16. USP 4,344,005
17. USP 4,403,158
18. USP 4,433,253
19. USP 4,442,481
20. USP 4,471,290

21. USP 4,486,670
22. USP 4,533,843
23. USP 4,543,500
24. USP 4,581,546
25. USP 4,583,157
26. USP 4,616,303
27. USP 4,621,315
28. USP 4,628,214
29. USP 4,639,622
30. USP 4,642,798
31. USP 4,656,373
32. USP 4,670,861
33. USP 4,689,504
34. USP 4,692,638
35. USP 4,697,252
36. USP 4,716,313
37. USP 4,730,132
38. USP 4,733,108
39. USP 4,740,918
40. USP 4,751,679
41. USP 4,798,977
42. USP 4,807,190
43. USP 4,811,304
44. USP 4,814,647
45. USP 4,820,941

46. USP 4,823,318

47. USP 4,837,462

48. USP 4,843,256

49. USP 4,857,763

50. USP 4,873,673

51. USP 4,878,201

52. USP 4,881,201

53. USP 4,888,738

54. USP 4,906,056

55. USP 4,951,259

56. USP 4,961,007

57. USP 5,010,259

58. USP 5,018,107

59. USP 5,023,465

60. USP 5,031,149

61. USP 5,038,325

62. USP 5,038,327

63. USP 5,059,815

64. USP 5,086,238

65. USP 5,101,381

66. USP 5,103,113

67. USP 5,150,325

68. USP 5,151,616

69. USP 5,159,215

70. USP 5,197,033

71. USP 5,208,776
72. USP 5,245,576
73. USP 5,262,999
74. USP 5,264,743
75. USP 5,276,646
76. USP 5,297,097
77. USP 5,307,315
78. USP 5,311,476
79. USP 5,323,354
80. USP 5,347,488
81. USP 5,351,217
82. USP 5,377,156
83. USP 5,751,643
84. USP 5,912,564
85. EP 0 010 137
86. EP 0 197 505
87. GB 2184902A
88. GB 2204456A
89. JP 56-62066
90. JP 59-213090
91. JP 60-161467
92. JP 61-17929
93. JP 61-30846
94. JP 62-178013
95. JP 63-292488

96. JP 3-23590

97. WO 86/04724

98. Ishihara et al., "256k CMOS Dynamic RAM with Static Column Mode of Cycle Time of 50ns," Nikkei Electronics, pp. 243-263 (2/11/85)

99. "An analysis of Toshiba TC511000/TC511001 CMOS 1Mx1 DRAMs," Mosaid Inc., 25 pages (Aug. 1986)

100. IBM Technical Disclosure Bulletin, "High Performance Complementary Decoder/Driver Circuit," V. 29, No. 6 (Nov. 1986)

101. IBM Technical Disclosure Bulletin, "Improved Decoder Circuits for CMOS Memory Arrays," V. 30, No. 2 (July 1987)

102. G. Kitsukawa et al., "An Experimental 1-Mbit BiCMOS DRAM," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5 (Oct. 1987)

103. Electronic Design, Vol. 36, No. 4, page 70 (2/18/88)

104. S. Fujii et al., "A 45ns 16Mb DRAM with Triple-Well Structure," 1989 IEEE International Solid-State Circuits Conference, pp. 248-249 (2/1989)

105. T. Watanabe et al., "Comparison of CMOS and BiCMOS 1-Mbit DRAM Performance," IEEE Journal of Solid-State Circuits, V. 24, No. 3, pp.771-778 (June 1989)

106. G. Kitsukawa et al. "A 1-Mbit BiCMOS DRAM Using Temperature-Compensation Circuit Techniques," IEEE Journal of Solid-State Circuits, Vol. 24, No. 3, pp. 597-601 (June 1989)

107. S. Fujii et al., "A 45ns 16Mb DRAM with Triple-Well Structure," IEEE Journal Of Solid-State Circuits, pp. 1170-1174 (Oct. 1989)

108. Y. Nakagomo et al., "A 1.5V Circuit Technology for 64 Mb DRAMs," 1990 Symposium on VLSI Circuits, pp. 17-18 (July 1990)

109. G. Kitsukawa et al. "A 23-ns 1-Mb BiCMOS DRAM," IEEE Journal of Solid-State Circuits, Vol. 25, No. 5, pp. 1102-1111 (Oct. 1990)

110. Y. Nakagome et al., "An Experimental 1.5V 64Mb DRAM," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, pp. 465-472 (Apr 1991)

111. P. Gillingham et al., "High-Speed High-Reliability Circuit Design for Megabit DRAM," IEEE Journal of Solid-State Circuits, Vol. 26, No. 8, pp. 1171-1175 (Aug. 1991)

112. Electronic Design, Vol. 40, No. 4, page 48 (2/20/92)

113. N.C.C. Lu et al., "A 20-ns 128-kbit x 4 High Speed DRAM with 330-Mbit/s Data Rate," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pp. 1140-1149 (October 1988)

114. M. Aoki et al., "A 1.5-V DRAM for Battery-Based Applications," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1206-1212 (October 1989)

115. M. Aoki et al., "New DRAM Noise Generation Under Half-Vcc Precharge and its Reduction Using a Transposed Amplifier," IEEE Journal of Solid-State Circuits, Vol. 24, No. 4, pp. 889-894 (August 1989)

116. K.Arimoto et al., "A 60-ns 3.3V-only 16-Mbit DRAM with Multipurpose Register," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1184-1189 (October 1989)

117. K. Arimoto et al., "A Speed-Enhanced DRAM Array Architecture with Embedded ECC," IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pp. 11-17 (February 1990)

118. M. Asakura et al., "An Experimental 1-Mbit Cache DRAM with ECC," IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pp. 3-10 (February 1990)

119. A.G. Eldin et al., "New Dynamic Logic and Memory Circuit Structures For BICMOS Technologies," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, pp. 450-453 (June 1987)

120. S. Fujii et al., "A 50-μA Standby 1M x 1 / 256k x 4 CMOS DRAM with High-Speed Sense Amplifier," IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 643-648 (October 1986)

121. T. Furuyama et al., "An Experimental 4-Mbit CMOS DRAM," IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 605-611 (October 1986)

122. R. Hori et al., "An Experimental 1 Mbit DRAM Based on High S/N Design," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 5, pp. 634-640 (October 1984)

123. P. Gray et al., "MOS Operational Amplifier Design – A Tutorial Overview," IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 6, pp. 969-982 (December 1982)

124. M. Horiguchi et al., "A Tunable CMOS-DRAM Voltage Limiter with Stabilized Feedback Amplifier," IEEE Journal of Solid-State Circuits, Vol. 25, No. 5, pp. 1129-1135 (October 1990)

125. K. Itoh, "Trends in Megabit DRAM Circuit Design," IEEE Journal of Solid-State Circuits, Vol. 25, No. 3, pp. 778-789 (June 1990)

126. K. Kimura et al., "A 65-ns 4-Mbit CMOS DRAM with a Twisted Driveline Sense Amplifier," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, pp. 651-656 (October 1987)

127. F. Matsoka et al., "A 256-Kbit Flash E^2PROM Using Triple-Polysilicon Technology," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 4, pp. 548-552 (August 1987)

128. J. Miyamoto et al., "An Experimental 5V-Only 256-Kbit CMOS EEPROM with a High Performance Single-Polysilicon Cell," IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 852-860 (October 1986)

129. M. Momodomi et al., "An Experimental 4_Mbit CMOS EEPROM with a NAND-Structured Cell," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1238-1243 (October 1989)

130. Y. Nakagome et al., "Circuit Techniques for 1.5-3.6V Battery-Operated 64-Mb DRAM," IEEE Journal of Solid-State Circuits, Vol. 26, No. 7, pp. 1003-1010 (July 1991)

131. K. Ohta et al., "A 1-Mbit DRAM with 33-MHz Serial I/O Ports," IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 649-654 (October 1986)

132. S. Saito et al., "A 1-Mbit CMOS DRAM with Fast Page Mode and Static Column Mode," IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 5, pp. 903-908 (October 1985)

133. G. Samachisa et al., "A 128K Flash EEPROM Using Double-Polysilicon Technology," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, pp. 676-683 (October 1987)

134. R. Scheuerlein et al., "Shared Word Line DRAM Cell," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 5, pp. 640-645 (October 1984)

135. M. Takada et al., "A 4-Mbit DRAM with Half-Internal-Voltage Bit-Line Precharge," IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, pp. 612-617 (October 1986)

136. T. Takeshima et al., "Voltage Limiters for DRAM's with Substrate-Plate-Electrode Memory Cells," IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, pp. 48-52 (February 1987)

137. J. Witters et al., "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1372-1380 (October 1989)

138. M. Horiguchi et al., "Dual-Operating-Voltage Scheme for a Single 5-V 16-Mbit DRAM," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pp. 1128-1132

(October 1988)

139. R. Scheuerlein et al., "Offset Word-Line Architecture for Scaling DRAM's to the Gigabit Level," IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, pp. 41-47 (February 1988)

140. "Analog MOS Integrated Circuits, II," Edited by P. Gray et al., IEEE Press (1989)

141. "Digital MOS Integrated Circuits II with Applications to Processors and Memory Design," M. Elmasry, IEEE Press (1992)

142. "Digital MOS Integrated Circuits Design for Applications," by Niantsu Wang, Prentice Hall.

143. "Memory Products Development 16Mbit DRAM Crib Notes," Texas Instruments Inc., July 1990.

144. Third Party Prior Art Devices including at least the Toshiba TC511000/TC511001 CMOS 1Mx1 DRAM, Micron 1M x 4 CMOS DRAM, Micron 1M DRAM, Micron 4M DRAM, (see Micron 000001 through Micron 000188), and Texas Instruments 64M DRAM.

The '602, '643, '253, and '640 patents are unenforceable for inequitable conduct committed during its procurement before the USPTO. Particularly, among other things, five material references were withheld during the prosecution of the '602 patent with an intent to deceive the USPTO. In an effort to obtain the patent by misleading the USPTO, the attorneys or others involved in prosecuting the application that eventually issued as the '602 patent and/or the inventor named on the '602 patent – Valerie L. Lines – knowingly and intentionally withheld and failed to disclose the following references to the USPTO: (1) Fujii, Syuso et al., "A 45-ns 16-Mbit DRAM with Triple-Well Structure," IEEE Journal of Solid State Circuits, vol. 24, no. 5, Oct. 1989, pp. 1170-1174; (2) N.C.C. Lu et al., "A 20-ns 128-kbit x 4 High Speed DRAM with 330-Mbit/s Data Rate," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, Oct. 1988, pp. 1140-1149; (3) US Patent No. 4,857,763; (4) US Patent No. 4,692,638; and (5) US Patent No. 4,583,157.. Mosaid knew of the withheld references during the prosecution of the '602 patent. The references are prior art to the '602 patent, and are material references, i.e., the USPTO

would have considered them important in its decision of whether to allow the '602 patent to issue.

The '643, '253, '640, '620, '201, and '581 patents (the "delayed patents") are unenforceable under the equitable defense of prosecution laches. Particularly, among other things, the claims of the delayed patents were first presented to the United States Patent and Trademark Office for examination after an unreasonable and inexcusable delay that caused injury to Samsung.

The '253 and '201 patents are invalid under the doctrine of double patenting. Particularly, at least one or more of claims of the '253 patent are invalid for obviousness-type and/or statutory-type double patenting over claims of the '643 patent. In addition, at least one or more claims of the '201 patent are invalid for obviousness-type and/or statutory-type double patenting over claims of the '620 patent.

The '602, '643, '253, and '640 patents are invalid for failure to set forth the best mode contemplated by the inventor of carrying out her invention. The inventor failed to disclose the high voltage Vpp supply embodied in the Sanyo Fast 1M DRAM and shown in U.S Application 07/680,994 filed on April 5, 1991. In addition, the '602, '253, and '640 patents are invalid for failure to set forth the best mode contemplated by the inventor for failing to disclose the secondary decoder circuit and hot electron protection devices and/or other circuit elements embodied in the Sanyo Fast 1M DRAM.

The '620, '201, and '581 patents are invalid for failure to set forth the best mode contemplated by the inventors of carrying out their invention. The inventor failed to disclose the decoder circuit embodied in the Sanyo Fast 1M DRAM and shown in U.S Application 07/680,746 filed on April 5, 1991. In addition, the '620, '201, and '581 patents are invalid for

failure to set forth the best mode contemplated by the inventors for failing to disclose the dual pump scheme to prevent excessive standby power, and/or other circuit elements embodied in the Sanyo Fast 1M DRAM..

The '643 patent is invalid because the inventor did not invent all the subject matter described in the specification that were represented by the inventor as inventive embodiments.

Samsung identifies the following as individuals having knowledge of the factual bases supporting Samsung's contentions:

1. Valerie L. Lines
2. Richard C. Foss
3. Peter B. Gillingham
4. Robert F. Harland
5. Michael Vladescu
6. Larry N. Anagnos
7. Donald R. Antonelli
8. Carl I. Brundidge
9. James N. Dresser
10. Melvin Kraus
11. Gregory E. Montone
12. Edward E. Pascal
13. Alan E. Schiavelli
14. James M. Smith
15. William I. Solomon

Samsung reserves the right to supplement this interrogatory response to include additional bases for invalidity and unenforceability.

INTERROGATORY NO. 4:

State in detail each of SAMSUNG's contentions that SAMSUNG does not infringe any claim of the MOSAID patents-in-suit, providing an identification of the documents that SAMSUNG contends supports such contentions, of the factual basis for such contentions, and of each person having knowledge of that factual basis.

RESPONSE TO INTERROGATORY NO. 4:

Subject to and without waiving its previously asserted general and specific objections, Samsung responds as follows:

Samsung's products do not infringe claim 1 of the '602 patent because, amongst other reasons, Samsung's products do not include at least a high V_{pp} supply voltage source which is in excess of high logic level V_{dd} plus one transistor threshold voltage but less than a transistor damaging voltage and the means for selecting the word line and means for having an input driven by the selecting means for applying the V_{pp} supply voltage level directly to the word line through the source-drain circuit of an FET, as required by the claim.

Samsung's products do not infringe claims 2-5 of the '602 patent because, amongst other reasons, Samsung's products do not infringe the claim(s) from which claims 2-5 depend. Further, Samsung's products do not infringe claim 2 because Samsung's products do not include at least the selecting means comprised of means for receiving V_{dd} level logic inputs and for providing an output to said applying means at V_{pp} logic levels, the level V_{pp} being higher than the supply voltage V_{dd}, as required by the claim. Further, Samsung's products do not infringe claim 3 because Samsung's products do not include at least the applying means comprised of a level shifter connected to the high supply voltage source having an output connected to the gate of a pass transistor whose source is connected to the high supply voltage source, the word line

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Valerie L. Lines

Continuation Application of

Application No.: 10/463,194

Filed: June 17, 2003

For: DYNAMIC MEMORY WORD LINE DRIVER SCHEME

Date: 3-2-04

EXPRESS MAIL LABEL NO. EV214952231US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Information Disclosure Statement is submitted under 37 CFR 1.97(b) before the mailing date of a first office action on the merits in a Continuation Application.

Attached is "Defendants' Second Supplemental Responses to Mosaid Technologies Incorporated's First Set of Interrogatories (2-4)," pages 1-13, filed by the Defendants in litigation in an infringement action based on patents to which this application claims priority. The response to Interrogatory 3 includes the Defendants' contentions with respect to validity of patents to which this application claims priority. The interrogatory response refers to patents by their final three digits. Those patent references correspond to the following patents, and those indicated by asterisks are patents to which this application claims priority:

'602	5,214,602*
'643	5,751,643*
'253	5,822,253*
'640	6,278,640*
'620	5,828,620
'201	6,055,201
'581	6,236,581

All of the references identified in that interrogatory response are being cited in this Information Disclosure Statement.

Also attached are the contentions of another Defendant, Infineon, with respect to patents to which this application claims priority. References cited in those contentions are also cited herein.

Other papers filed by the Defendants can be found in parent application 09/919,752, now U.S. patent 6,603,703.

Enclosed herewith is form PTO-1449 and copies of all foreign patent documents and other documents are attached. Since this application was filed after June 30, 2003, copies of issued U.S. patents and published U.S. applications are not required and are not being provided.

It is requested that the information disclosed herein be made of record in this application.

Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
James M. Smith
Registration No.: 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 3/2/4

PTO-1449 REPRODUCED	ATTORNEY DOCKET NO. 2037.1006-012	CONT. OF APPLICATION NO. 10/463,194	
INFORMATION DISCLOSURE CITATION IN AN APPLICATION	APPLICANT Valerie L. Lines		
March 2, 2004	FILING DATE	CONFIRMATION NO.	GROUP
(Use several sheets if necessary)			

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER	ISSUE DATE / PUBLICATION DATE	NAME
	AA	4,189,782	02/19/1980	Dingwall
	AB	4,442,481	04/10/1984	Brahmbhatt
	AC	4,583,157	04/15/1986	Kirsch et al.
	AD	4,689,504	08/25/1987	Raghunathan et al.
	AE	4,692,638	09/08/1987	Stiegler
	AF	4,716,313	12/29/1987	Hori et al.
	AG	4,730,132	03/08/1988	Watanabe et al.
	AH	4,814,647	03/21/1989	Tran
	AI	4,857,763	08/15/1989	Sakurai et al.
	AJ	4,878,201	10/31/1989	Nakaizumi
	AK	4,888,738	12/19/1989	Wong et al.
	AA2	5,010,259	04/23/1991	Inoue et al.
	AB2	5,031,149	07/09/1991	Matsumoto et al.
	AC2	5,038,327	08/06/1991	Akaogi
	AD2	5,150,325	09/22/1992	Yanagisawa et al.
	AE2	5,347,488	09/13/1994	Matsusbita
	AF2	5,351,217	09/27/1994	Jeon
	AG2	5,377,156	12/27/1994	Watanabe et al.
	AH2	4,814,647	03/21/1989	Tran
	AI2	5,031,149	07/09/1991	Matsumoto et al.
	AJ2	5,038,327	08/06/1991	Akaogi
	AK2	5,751,643	05/12/1998	Lines
	AA3	4,344,005	08/10/1982	Stewart
	AB3	5,023,465	06/11/1991	Douglas et al.
	AC3	3,801,831	04/02/1974	Dame
	AD3	3,942,047	03/02/1976	Buchanan

EXAMINER	DATE CONSIDERED

PTO-1449 REPRODUCED	ATTORNEY DOCKET NO.	CONT. OF APPLICATION NO.	
INFORMATION DISCLOSURE CITATION IN AN APPLICATION	2037.1006-012	10/463,194	
	APPLICANT Valerie L. Lines		
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER	ISSUE DATE / PUBLICATION DATE	NAME
	AE3	3,980,899	09/14/1976	Shimada et al.
	AF3	4,000,412	12/28/1976	Rosenthal et al.
	AG3	4,039,862	08/02/1977	Dingwall et al.
	AH3	4,080,539	03/21/1978	Stewart
	AI3	4,208,595	06/17/1980	Gladstein
	AJ3	4,271,461	06/02/1981	Hoffmann et al.
	AK3	4,279,010	07/14/1981	Morihisa
	AA4	4,307,333	12/22/1981	Hargrove
	AB4	4,403,158	09/06/1983	Slemmer
	AC4	4,433,253	02/21/1984	Zapisek
	AD4	4,486,670	12/04/1984	Chan et al.
	AE4	4,543,500	09/24/1985	McAlexander, et al.
	AF4	4,581,546	04/08/1986	Allan
	AG4	4,621,315	11/04/1986	Vaughn et al.
	AH4	4,628,214	12/09/1986	Leuschner
	AI4	4,642,798	02/10/1987	Rao
	AJ4	4,656,373	04/07/1987	Plus
	AK4	4,670,861	06/02/1987	Shu et al.
	AA5	4,697,252	09/29/1987	Furuyama et al.
	AB5	4,730,132	03/08/1988	Watanabe et al.
	AC5	4,740,918	04/26/1988	Okajima et al.
	AD5	4,751,679	06/14/1988	Dehganpour
	AE5	4,798,977	01/17/1989	Sakui et al.
	AF5	4,807,190	02/21/1989	Ishii et al.
	AG5	4,811,304	03/07/1989	Matsuda et al.

EXAMINER	DATE CONSIDERED

PTO-1449 REPRODUCED	ATTORNEY DOCKET NO.	CONT. OF APPLICATION NO.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER	ISSUE DATE / PUBLICATION DATE	NAME
	AH5	4,837,462	06/06/1989	Watanabe et al.
	AI5	4,843,256	06/27/1989	Scade et al.
	AJ5	4,873,673	10/10/1989	Hori et al.
	AK5	4,881,201	11/14/1989	Sato et al.
	AA6	4,906,056	03/06/1990	Taniguchi
	AB6	4,951,259	08/21/1990	Sato et al.
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